Amendments to the Claims

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A frequency synthesizer having a phase locked loop, comprising:

a controllable oscillator having an output frequency dependent upon a plurality of different analog control signals, the plurality of different analog control signals being received by the controllable oscillator as different frequency control input signals such that at least some of the plurality of control signals are configured to individually control the output frequency of the controllable oscillator without being combined with others of the plurality of control signals;

a phase detector configured to concurrently provide a plurality of different analog output signals, the plurality of different analog output signals being generated from a phase difference between at least two input signals; and

a sample and hold circuit coupled to sample each of the ~~different~~ plurality of different analog output signals from the phase detector and to hold a plurality of different sampled analog output signals, the plurality of different sampled analog output signals from the sample and hold circuit being used to provide the plurality of different analog control signals for the controllable oscillator.

4. (Previously Presented) The frequency synthesizer of claim 3, wherein the input signals to the phase detector comprise a first input signal coupled to an output of the controllable oscillator and a second input signal coupled to a reference signal.

5. (Previously Presented) The frequency synthesizer of claim 3, wherein the input signals to the phase detector comprise a plurality of first input signals based upon an output of the controllable oscillator and at least one other second input signal coupled to a reference signal, the plurality of analog output signals

being generated from the phase differences between the plurality of first input signals and the at least one other second input signal.

6. (Previously Presented) The frequency synthesizer of claim 5, wherein the number of first input signals and the number of analog output signals is equal.

7. (Previously Presented) The frequency synthesizer of claim 5, wherein the number of analog output signals is at least five.

8. (Previously Presented) The frequency synthesizer of claim 5, wherein the number of analog output signals is at least twenty.

9. (Previously Presented) The frequency synthesizer of claim 5, wherein the plurality of first input signals are signals having at least one phase shifted edge with respect to each other.

10. (Previously Presented) The frequency synthesizer of claim 9, further comprising a shift register having the plurality of phase shifted signals as outputs.

11. (Previously Presented) The frequency synthesizer of claim 5, wherein the phase detector comprises a plurality of phase detector sub-circuits, each sub-circuit having as an output one of the plurality of analog output signals and having as inputs at least one of the plurality of first signals and at least one of the second signals.

12. (Currently Amended) Phase locked loop circuitry for generating an output signal at a variable output frequency, comprising:

a controllable oscillator having an output signal at an output frequency dependent upon a plurality of different analog control signals, the plurality of different analog control signals being received by the controllable oscillator as different frequency control input signals such that at least some of the plurality of analog control signals are configured to individually control the output frequency of the controllable oscillator without being combined with others of the plurality of analog control signals; and

phase difference control circuitry configured to concurrently provide the plurality of different analog control signals as outputs, the plurality of different analog control signals being generated from a phase difference between at least two input signals;

wherein the controllable oscillator comprises a plurality of non-varactor diode capacitance circuits connected in parallel to contribute a combined capacitance amount that determines at least in part the output frequency of the controllable oscillator, the plurality of different analog control signals from the phase difference control circuitry being coupled to control the amount of capacitance contributed by the plurality of capacitance circuits.

13. (Previously Presented) The phase locked loop circuitry of claim 12, wherein the phase difference control circuitry comprises a phase detector configured to receive the at least two input signals and to output a plurality of different analog output signals based upon phase differences and sample-and-hold circuitry configured to receive the plurality of different analog output signals and to output the plurality of different analog control signals.

14. (Previously Presented) The phase locked loop circuitry of claim 12, wherein the controllable oscillator comprises an LC tank resonant structure including the plurality of capacitance circuits.

15. (Previously Presented) The phase locked loop circuitry of claim 12, wherein the each of the plurality of capacitance circuits comprises at least one capacitor and a variable resistance element, the variable resistance element being coupled to at least one of the plurality of analog control signals.

16. (Previously Presented) The phase locked loop circuitry of claim 15, wherein the variable resistance element comprises a transistor and wherein at least one capacitor is coupled to the source or drain of the transistor and the control signal is coupled to the gate of the transistor.

17. (Previously Presented) The phase locked loop circuitry of claim 16, further comprising at least a second capacitor coupled between the source and drain of the transistor.

18. (Previously Presented) The phase locked loop circuitry of claim 12, wherein at least one of the input signals to the phase difference control circuitry is adjustable and is configured to determine at least in part the frequency of the output signal.

19. (Previously Presented) The phase locked loop circuitry of claim 18, wherein one input signal to the phase difference control circuitry is an adjustably divided version of the output signal and a second input signal to the phase difference control circuitry is an adjustably divided version of a reference signal, the first and second .

20. (Currently Amended) A method of operating phase locked loop circuitry for generating an output signal at a variable output frequency, comprising:

controlling an output frequency of a controllable oscillator utilizing at least in part a plurality of different analog control signals, the plurality of different analog control signals being received by the controllable oscillator as different frequency control input signals such that at least some of the plurality of analog control signals are configured to individually control the output frequency of the controllable oscillator without being combined with others of the plurality of analog control signals; and

detecting a phase difference between at least two input signals with phase difference control circuitry to concurrently provide the plurality of different analog control signals as outputs;

wherein the controllable oscillator comprises a plurality of non-varactor diode capacitance circuits connected in parallel to contribute a combined capacitance amount that determines at least in part the output frequency of the controllable oscillator, the plurality of different analog control signals from the phase difference control circuitry being coupled to control the amount of capacitance contributed by the plurality of capacitance circuits.

21. (Previously Presented) The method of 20, wherein the detecting step comprises detecting a phase difference between at least two input signals, generating a plurality of different analog output signals based upon phase differences, sampling the plurality of different analog output signals, and holding a plurality of sampled analog output signals to provide the plurality of different analog control signals.

22. (Previously Presented) The method of claim 20, wherein the controllable oscillator comprises an LC tank resonant structure including the plurality of capacitance circuits.

23. (Previously Presented) The method of claim 20, wherein the each of the plurality of capacitance circuits comprises at least one capacitor and a variable resistance element, the variable resistance element being coupled to at least one of the plurality of analog control signals.

24. (Previously Presented) The method of claim 23, wherein the variable resistance element comprises a transistor, wherein at least one capacitor is coupled to the source or drain of the transistor, and wherein the control signal is coupled to the gate of the transistor.

25. (Previously Presented) The method of claim 20, further comprising adjusting at least one of the input signals to the phase difference control circuitry to determine at least in part the frequency of the output signal.

26. (Previously Presented) The method of claim 25, wherein one input signal to the phase difference control circuitry is an adjustable divided version of the output signal and a second input signal to the phase difference control circuitry is an adjustable divided version of a reference signal, the first and second .